IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the present application:

1. (Currently amended) A transport processor comprising:

a front end to receive ~~multiple~~ concurrently a plurality of transport streams, where two or more of the plurality of transport streams can have different formats, each transport stream including a plurality of packets, the front end comprising a packet processor to create an aggregate transport stream in a single format from the plurality of transport streams; and

a memory ~~to~~ interface through which the transport processor can store the aggregate transport stream in a memory for ~~subsequent processing~~use by subsequent decode and display operations.

2. (Original) The transport processor of claim 1, wherein the number of streams within the aggregate transport stream is scaleable.

3. (Original) The transport processor of claim 1, wherein the front end further comprises:

a PID filter to discard packets in the aggregate transport stream prior to processing, in order to minimize memory bandwidth and improve descrambling and demultiplexing throughput.

4. (Original) The transport processor of claim 1, wherein the aggregation of transport streams permits the use of a single PID filter, a single descrambler, and a single demultiplexer.

5. (Original) The transport processor of claim 1, further comprising:

a descrambler to descramble the packets in the aggregate transport stream.

6. (Currently amended) The ~~descrambler in the~~ transport processor of claim 5, ~~further comprising~~wherein the descrambler comprises:

a packet level control and key RAM control logic to select a descrambling standard for a packet within the aggregate transport stream; and

a decryption circuit to descramble the packet using the selected descrambling standard.

7. (Currently amended) The transport processor of claim 1, ~~further comprising~~wherein:

the packet processor further is to format each packet from ~~multiple~~ the plurality of transport streams to ~~a common~~said single format prior to storing the aggregate transport stream in the memory~~, the common format including originating stream information~~.

8. (Currently amended) The transport processor of claim 7, wherein the ~~common~~ single format is a 208-byte format, and ~~smaller~~ packets with fewer than 208 bytes are padded to ~~create this common~~comply with the single format.

9. (Currently amended) The transport processor of claim 7, wherein the single format includes originating stream information that comprises temporal information.

10. (Currently amended) The transport processor of claim 7, wherein the single format includes originating stream information that comprises stream identifier and additional user specified information.

11. (Original) The transport processor of claim 1, wherein the aggregate stream includes transport data obtained from different transport protocol standards.

12. (Original) The transport processor of claim 1, further comprising:

a plurality of input/output (I/O) ports;

an I/O port that is user-selectable to a parallel or serial format.

13. (Currently amended) The ~~I/O ports in the~~ transport processor of claim 12, ~~further comprising~~wherein the I/O ports comprise:

a serial output block to resample parallel data, and to convert the parallel data to serial data with an independently programmable bit clock selection.

14. (Original) The transport processor of claim 1, further comprising:

a PID filter to discard packets from the aggregate transport stream, retaining only packets of interest;

a descrambler to descramble the remaining packets in the aggregate stream; and

a demultiplexer to demultiplex the descrambled packets in the aggregate stream;

wherein the descrambler and the demultiplexer receive only the packets of interest.

15. (Original) The transport processor of claim 1, further comprising:

a switching matrix to select a subset of the streams out of a plurality of streams for storage and subsequent descrambling and demultiplexing.

16. (Currently amended) The ~~switching matrix in the~~ transport processor of claim 15, ~~further comprising~~wherein the switching matrix comprises:

a delay circuit to switch to a new stream after receiving an end of packet signal from an original stream, such that only complete packets from the original stream are propagated.

17. (Currently amended) The ~~switching matrix in the~~ transport processor of claim 16, wherein the switching matrix further ~~comprising~~comprises:

a data valid signal to indicate that the output of the switching matrix is valid only after an end of packet signal is received from the new stream, such that only complete packets from the new stream are propagated.

18. (Currently amended) A system on a chip (SOC) comprising:

a transport processor to PID filter, descramble, and demultiplex a plurality of transport streams, the transport processor including

a front end to receive a plurality of transport streams, where two or more of the transport streams can have different formats, and

a packet processor to create an aggregate transport stream having a single format from the plurality of transport streams;

a memory to store demultiplexed outputs of the plurality of transport streams; and

an output processor to retrieve one or more demultiplexed outputs from the memory and perform audio/video decode and display functions simultaneously.

19. (Original) The SOC of claim 18, wherein the output processor is a combination of digital audio decoder, digital video decoder, audio processor, and display processor.

20. (Original) The SOC of claim 19, wherein the audio and video frames for two independent transport streams are rendered without repeated or skipped frames.

21. (Currently amended) The SOC of claim 18, wherein the transport processor further comprises:

~~a front end to receive multiple transport streams, each transport stream including a plurality of packets, the front end comprising a packet processor to create an aggregate transport stream; and~~

a readback logic to read packets from the memory, for descrambling and demultiplexing functions.

22. (Currently amended) The SOC of claim 18, further comprising a memory interface ~~to access the contents of the memory, the memory interface used~~ for use by the transport processor and the output processor to access contents of the memory.

23. (Currently amended) A front end in a transport processor to receive a plurality of transport streams from digital receivers, comprising:

a switching matrix to receive concurrently the plurality of transport streams, where two or more of the plurality of transport streams can have different formats, and to output a programmable subset of the plurality of transport streams;

a packet processor to receive the subset of the plurality of transport streams and to aggregate the subset of the plurality of streams into a single aggregate transport stream in a single format.

24. (Original) The front end of claim 23, further comprising:

a memory to store the aggregate transport stream.

25. (Original) The front end of claim 24, further comprising:

a PID filter to discard packets, retaining only packets of interest.

26. (Original) The front end of claim 24, further comprising:

an external input/output (I/O) to receive the plurality of transport streams, the external I/O having a plurality of bi-directional ports.

27. (Original) The front end of claim 26, wherein each of the bi-directional ports can be configured as either a single parallel or a pair of serial ports.

28. (Original) The front end of claim 27, wherein a bi-directional port includes a serial input block to receive serial input and generate a synchronized parallel output.

29. (Original) The front end of claim 27, wherein a bi-directional port includes a serial output block to generate a serial transport stream with an independent bit clock for output.

30. (Original) The front end of claim 23, wherein the switching matrix comprises:

a stream select delay unit to ensure that only compete packets are propagated.

31. (Original) The front end of claim 23, wherein the packet processor is further to attach appropriate header and footer information to transport packets in the subset of the plurality of transport streams.

32. (Original) The pocket processor in the front end of claim 31, wherein the packet processor generates packets of a uniform size, regardless of originating protocol.

33. (New) The transport processor of claim 1, further comprising:

a demultiplixer to demultiplex an aggregate transport stream retrieved from the memory, into a plurality of different streams, for use by said decode and display operations.

34. (New) The transport processor of claim 33, further comprising a descrambler to receive the aggregate transport stream from the memory via the memory interface and to provide a descrambled version of the aggregate transport stream to the demultiplexer.

35. (New) The transport processor of claim 7, wherein the single format includes originating stream information.

36. (New) A digital audio/video receiver system comprising,

on a single chip:

a transport processor including

a front end, the front end including:

a switching matrix to receive concurrently a plurality of transport streams, including video and audio, each including a plurality of packets, where two or more of the plurality of transport streams can have different media formats, each transport stream including a plurality of packets,

a PID filter to filter out packets that do not meet specified criteria, and

a packet processor to create an aggregate transport stream in a single format from the plurality of transport streams;

a memory interface through which the transport processor can store the aggregate transport stream in a memory for subsequent processing;

a descrambler to descramble packets read from the memory, and

a demultiplixer to demultiplex packets read from the memory, for use by subsequent decode and display operations;

a digital decoder to perform video processing functions including decompression of video received from the memory and to store processed video in the memory;

an audio processor to perform audio processing functions including audio decompression on audio received from the memory and to generate an audio output of said digital audio/video receiver system;

a graphics processor to process graphics; and

a display processor to produce a display output of said digital audio/video receiver system by combining processed graphics and video from a plurality of sources to generate a display in any of a plurality of different display formats.

37. (New) A method comprising:

receiving concurrently, in a digital audio/video receiver system, a plurality of transport streams which have a plurality of different formats, each transport stream including a plurality of packets;

creating an aggregate transport stream in a single format from the plurality of transport streams in said digital audio/video receiver system; and

storing the aggregate transport stream in a memory for use by subsequent decode and display operations.

38. (New) The method of claim 37, further comprising:

demultiplexing an aggregate transport stream retrieved from the memory into a plurality of different streams, for use by said decode and display operations.

39. (New) The method of claim 38, further comprising:

descrambling the aggregate transport stream retrieved from the memory.